THE UNITED STATES PATENT AND TRADEMARK OFFICE

**INFORMATION DISCLOSURE STATEMENT**

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| APPLICANT: | Gabric et al | |
| SERIAL NO.: | 10/606,069 | GROUP ART UNIT: 2812 |
| FILED: | June 25, 2003 | CONFIRMATION NO.: 1618 |
| INVENTION: | "METHOD FOR FABRICATING MICROSTRUCTURES AND ARRANGEMENT OF MICROSTRUCTURES" | |

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

S I R:

In accordance with the provisions of 37 CFR 1.56, 1.97 and 1.98, it is requested that a citation and examination of the references listed on the attached Form PTO-1449 be made during the course of the examination of the above-identified application.

**REMARKS**

In the Background of the Invention, on pages 1, 2 and 3 of the application, U.S. Patent Nos. 5,821,014; 5,869,880; 5,936,295; 6,083,275; 6,252,290; 6,277,728 and 6,297,125 were cited and discussed. Copies of these seven U.S. Patents are attached herewith.

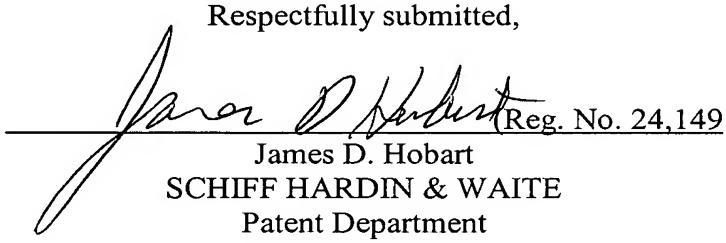
Also discussed in the Background of the Invention were German 199 57 302 and its corresponding United States Patent Application Publication No. US 2001/0002732 A1 and German 101 09 778. Copies of these two German Applications plus the United States Patent Application Publication are also attached herewith.

In addition to these patent references, the first page of the application, in the Background of the Invention, cites and discusses an article by Bohr, an article by S. Oh and K. Chang, an article by T.H. Ning and an article by K. Yamashita and S. Odanaka. Copies of these four articles are also attached herewith.

It is respectfully submitted that the specification distinguishes the method of claims 1-16 and the arrangement of microstructures recited in claims 17-24 from the teachings of the above-identified 14 references.

In a German Office Action dated February 5, 2003 for the corresponding German Application DE 102 28 344.3, from which the present application claims priority, the above-mentioned U.S. Patent No. 5,869,880 was cited along with EP 1 152 463 and an article by Ueda et al entitled "A Novel Air Gap Integration Scheme for Multi-Level Interconnects Using Self-Aligned Via Plugs". A copy of the article and the European Application are also attached herewith. It is respectfully submitted that the claims of the present application are patentable over the teachings of these two references and are allowable.

Respectfully submitted,



Reg. No. 24,149

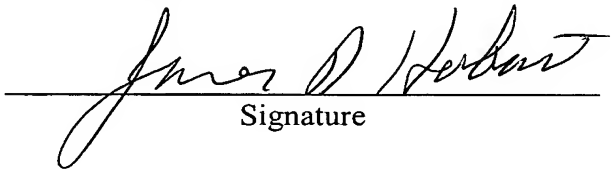
James D. Hobart
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
(312) 258-5781
**Customer Number: 26574**

DATED: October 1, 2003

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450 on October 1, 2003.

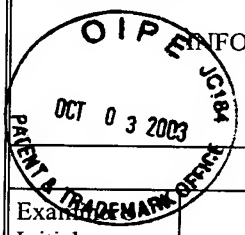
James D. Hobart
Name of Applicants' Attorney



Signature

October 1, 2003
Date

Form PTO-1449




INFORMATION DISCLOSURE CITATION IN AN APPLICATION
(use several sheets if necessary)

| Docket No. P03,0217 | Serial No. 10/606,069 |
|---|---|
| Applicant Gabric et al | |
| Filing Date June 25, 2003 | Group Art Unit 2812 |

**U.S. PATENT DOCUMENTS**

| Examiner Initials | | Document Number | Date | Name | Class | Subclass | Filing Date If appropriate |
|---|---|---|---|---|---|---|---|
| | AA | 5,821,014 | 10/13/1998 | Chen et al | | | |
| | AB | 5,869,880 | 02/09/1999 | Grill et al | | | |
| | AC | 5,936,295 | 08/10/1999 | Havemann et al | | | |
| | AD | 6,083,275 | 07/04/2000 | Heng et al | | | |
| | AE | 6,252,290 | 06/26/2001 | Quek et al | | | |
| | AF | 6,277,728 | 08/21/2001 | Ahn et al | | | |
| | AG | 6,297,125 | 10/02/2001 | Nag et al | | | |
| | AH | | | | | | |
| | AI | | | | | | |

**FOREIGN PATENT DOCUMENTS**

| | | Document Number | Date | Country | Class | Subclass | Translation | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Yes | No |
| | AJ | 1 152 463 | 11/07/2001 | Europe | | | | |
| | AK | 199 57 302 | 05/31/2001 | Germany | | | See AP | |
| | AL | 101 09 778 | 09/19/2002 | Germany | | | | X |
| | AM | | | | | | | |
| | AN | | | | | | | |
| | AO | | | | | | | |

**OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | | |
|---|---|---|
| | AP | United States Patent Application Publication no. US 2001/0002732 of Schwarzl et al, published June 7, 2001 |
| | AQ | M.T. Bohr, "Interconnect Scaling – The Real Limiter to High Performance ULSI", IEDM 95, pages 241 – 244 |
| | AR | S. Oh and K. Chang, "2001 Needs for Multi-Level Interconnect Technology", Circuits & Devices, January 1995, pages 16 – 20 |
| | AS | T.H. Ning, "0.1 μm Technology and BEOL", Mat. Res. Soc. Symp. Proc., Vol. 427, 1996, pages 17 – 21 |
| | AT | K. Yamashita & S. Odanaka, "Interconnect Scaling Scenario using a Chip Level Interconnect Model", Symp. On VLSI Technology Digest of Technical Papers, 1997, pages 53 - 54. |
| | AU | Ueda et al, "A Novel Air Gap Integration Scheme for Multi-Level Interconnects Using Self-Aligned Via Plugs", 1998 Symposium on VLSI Technology Digest of Technical Papers, pp 46, 47. |

| Examiner | Date Considered |
|---|---|
| | |

***EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**